What is claimed is:

1. A method of designing a custom circuit device, which begins with a high level architecture of subsystems coupled by virtual wires, comprising the steps of:

spatially placing the subsystems onto tiles;

routing the virtual wires that cross boundaries of the tiles onto an interconnect architecture, the interconnect architecture comprising switches and registers such that some of the switches route a signal from a first subsystem located on a first tile to a second subsystem located on a second tile and further such that at least two of the registers consecutively latch the signal at a time interval of no more than a repeating time period; and

scheduling of tasks according to clock cycles.

2. The method of claim 1 wherein the repeating time period comprises a clock cycle period.

3. The method of claim 1 wherein the repeating time period comprises a multiple of clock cycle periods.

4. The method of claim 1 further comprising the step of mapping the subsystems and the virtual wires that do not cross the boundaries of the tiles onto circuits of the tiles.

5. The method of claim 1 wherein the subsystems comprise virtual entities.

6. The method of claim 5 wherein the virtual entities comprise operations and memory objects.

7. The method of claim 1 wherein the subsystems comprise hardware entities.

8. The method of claim 7 wherein the hardware entities comprise functional units.

9. The method of claim 7 wherein the hardware entities comprise memory blocks.

10. The method of claim 1 wherein the step of spatially placing the subsystems onto the tiles seeks optimization of communication between the subsystems located on different tiles.

11. The method of claim 10 wherein the optimization of the communication between the subsystems located on the different tiles seeks to minimize communication distances for critical communication paths.

12. The method of claim 10 wherein the optimization of the communication between the subsystems located on different tiles seeks efficient use of communication paths by sharing of communication path segments by signals.

13. The method of claim 12 wherein the communication comprises time multiplexing of the signals.

14. The method of claim 12 wherein the communication comprises transmission of first and second signals during different time segments.

15. The method of claim 10 wherein the optimization of the communication between the subsystems located on different tiles seeks efficient use of communication paths by not sharing of communication path segments by signals.

16. The method of claim 1 wherein the step of scheduling of the tasks comprises accounting for latencies caused by communication between the tiles.

17. The method of claim 1 wherein the step of scheduling of the tasks comprises ensuring that no communication path segment of the interconnect architecture exceeds its capacity.

18. The method of claim 1 wherein the step of scheduling of the tasks comprises generating an overall schedule of operations comprising subsystem tasks and

communications between the tiles.

19. The method of claim 1 wherein the step of spatially placing the subsystems onto the tiles begins before the step of routing the virtual wires onto the interconnect architecture.

20. The method of claim 1 wherein the steps of spatially placing the subsystems onto the tiles and routing the virtual wires onto the interconnect architecture overlap in time.

21. The method of claim 1 wherein the steps of spatially placing the subsystems onto the tiles and routing the virtual wires onto the interconnect architecture do not overlap in time.

22. The method of claim 1 wherein the custom circuit device comprises an application specific integrated circuit.

23. The method of claim 1 wherein the custom circuit device comprises a reconfigurable device.

24. The method of claim 23 wherein the reconfigurable device comprises a field programmable gate array.

25. The method of claim 23 wherein the tiles of the reconfigurable device comprise virtual tiles and further wherein the interconnect architecture of the reconfigurable device comprises a virtual interconnect architecture.

26. The method of claim 25 further comprising the steps of allocating resources of the reconfigurable device to the virtual tiles and allocating other resources to the virtual interconnect architecture.

27. The method of claim 23 wherein the tiles of the reconfigurable device comprise real tiles and further wherein the interconnect architecture comprises a real interconnect architecture.

28. The method of claim 27 wherein a physical design of the reconfigurable device comprises the real tiles and the real interconnect architecture.

29. A method of designing a custom circuit device, which begins with a high level architecture of subsystems coupled by virtual wires, comprising the steps of:

spatially placing the subsystems onto tiles, thereby forming subsystem placements, each of the tiles comprising a circuit;

routing the virtual wires that cross boundaries of the tiles onto an interconnect architecture, the interconnect architecture comprising switches and registers such that some of the switches route a signal from a first subsystem located on a first tile to a second subsystem located on a second tile and further such that at least two of the registers consecutively latch the signal at a time interval of no more than a repeating time period;

scheduling of tasks according to clock cycles; and

mapping the subsystems and the virtual wires that do not cross the boundaries of the tiles onto the circuits of the tiles according to the subsystem placements.

30. The method of claim 29 wherein the repeating time period comprises a clock cycle period.

31. The method of claim 29 wherein the repeating time period comprises a multiple of clock cycle periods.

32. A method of designing a custom circuit device, which begins with a high level architecture of subsystems coupled by virtual wires, comprising the steps of:

spatially placing the subsystems onto tiles;

routing the virtual wires that cross boundaries of the tiles onto an interconnect architecture, the interconnect architecture comprising switches and registers such that some of the switches route a signal from a first subsystem located on a first tile to a second subsystem located on a second tile and further such that at least two of the registers consecutively latch the signal at a time interval of no more than a clock cycle period; and

scheduling of tasks according to clock cycles.

33. A computer readable memory comprising computer code for implementing a method of designing a custom circuit device, which begins with a high level architecture of subsystems coupled by virtual wires, the method of designing the custom circuit device comprising the steps of:

spatially placing the subsystems onto tiles;

routing the virtual wires that cross boundaries of the tiles onto an interconnect architecture, the interconnect architecture comprising switches and registers such that some of the switches route a signal from a first subsystem located on a first tile to a second subsystem located on a second tile and further such that at least two of the registers consecutively latch the signal at a time interval of no more than a repeating time period; and

scheduling of tasks according to clock cycles.

34. A computer readable memory comprising computer code for implementing a method of designing a custom circuit device, which begins with a high level architecture of subsystems coupled by virtual wires, the method of designing the custom circuit device comprising the steps of:

spatially placing the subsystems onto tiles, thereby forming subsystem placements, each of the tiles comprising a circuit;

routing the virtual wires that cross boundaries of the tiles onto an interconnect architecture, the interconnect architecture comprising switches and registers such that some of the switches route a signal from a first subsystem located on a first tile to a second subsystem located on a second tile and further such that at least two of the registers consecutively latch the signal at a time interval of no more than a repeating time period;

scheduling of tasks according to clock cycles; and

mapping the subsystems and the virtual wires that do not cross the boundaries of the tiles onto the circuits of the tiles according to the subsystem placements.

35. A computer readable memory comprising computer code for implementing a

method of designing a custom circuit device, which begins with a high level architecture of subsystems coupled by virtual wires, the method of designing the custom circuit device comprising the steps of:

spatially placing the subsystems onto tiles;

routing the virtual wires that cross boundaries of the tiles onto an interconnect architecture, the interconnect architecture comprising switches and registers such that some of the switches route a signal from a first subsystem located on a first tile to a second subsystem located on a second tile and further such that at least two of the registers consecutively latch the signal at a time interval of no more than a clock cycle period; and

scheduling of tasks according to clock cycles.